

FIG. 1

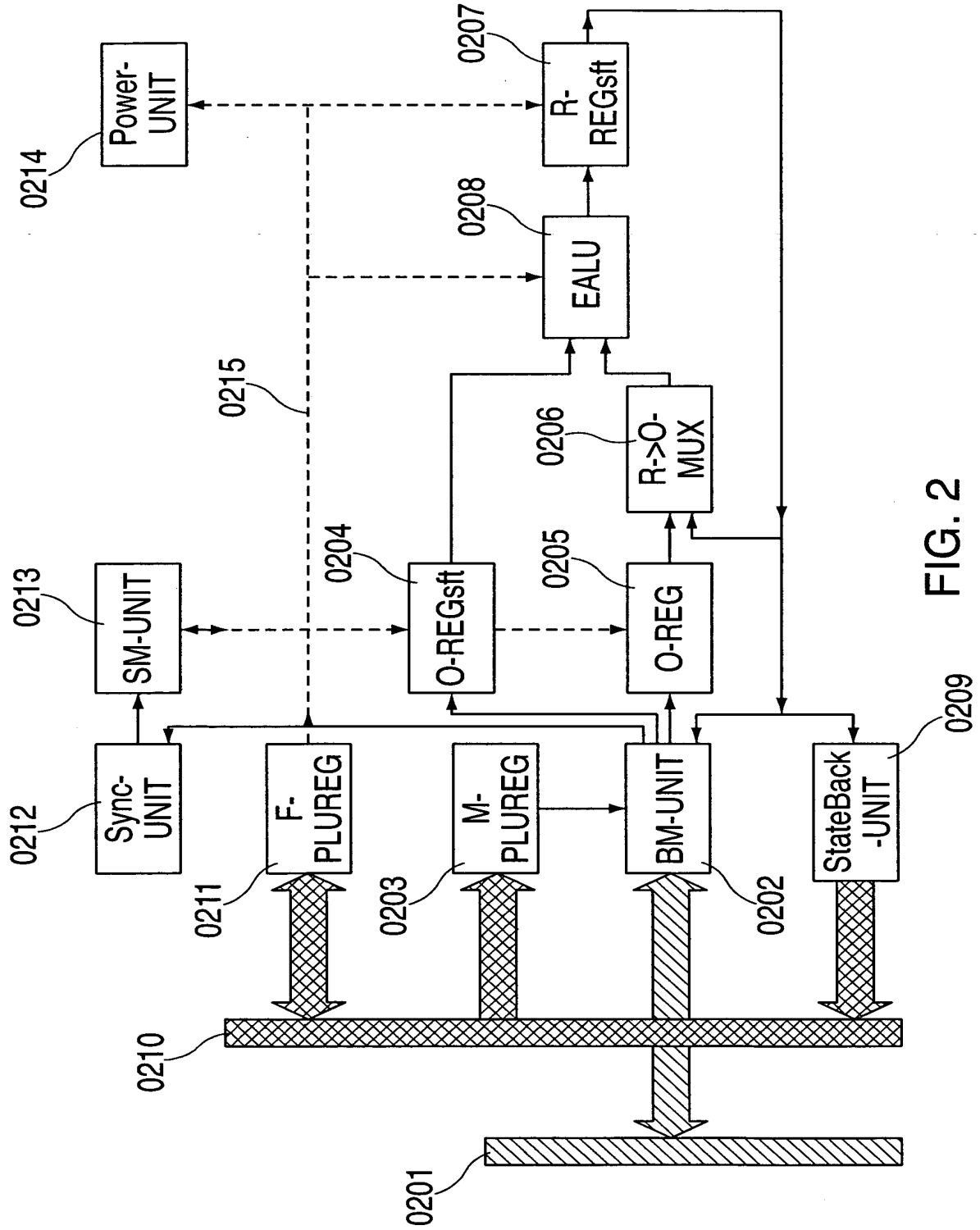


FIG. 2

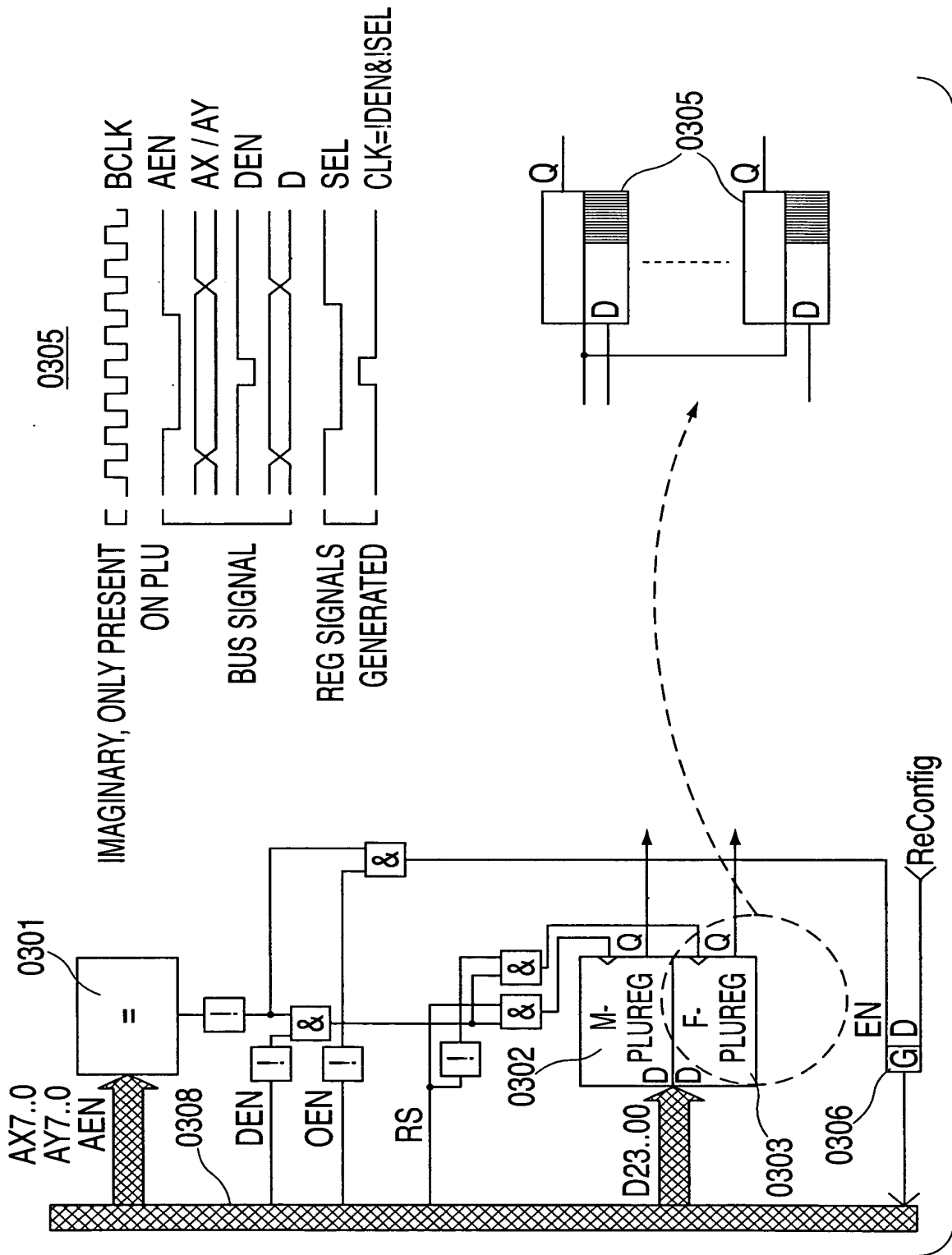


FIG. 3

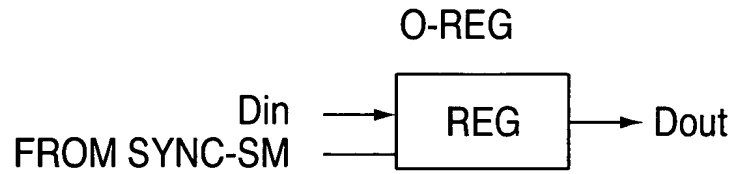


FIG. 4a

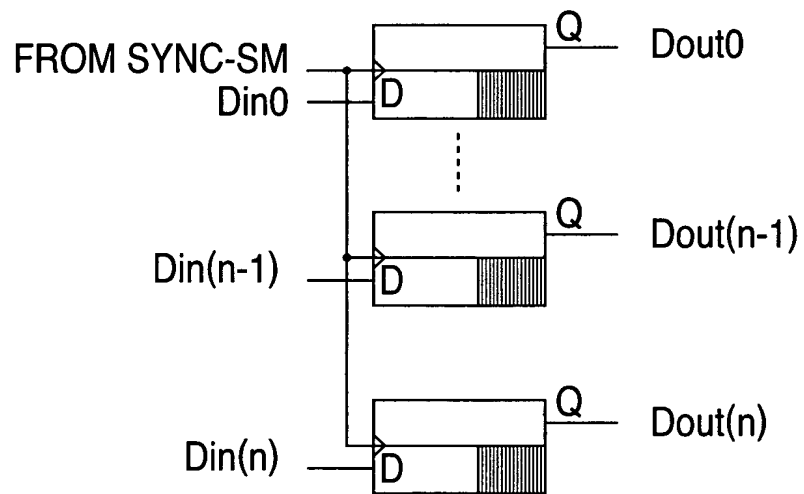


FIG. 4b

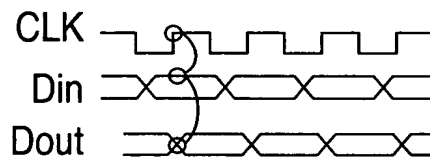


FIG. 4c

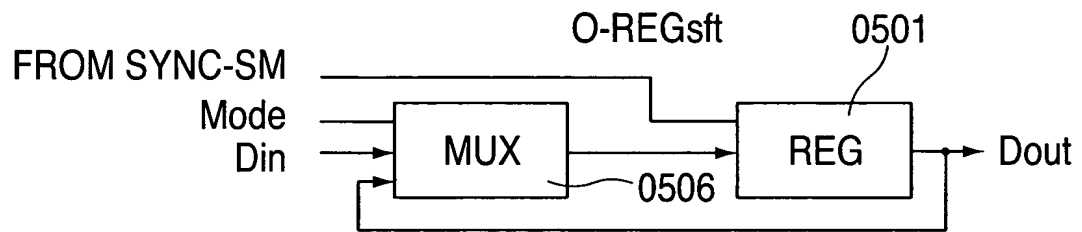


FIG. 5a

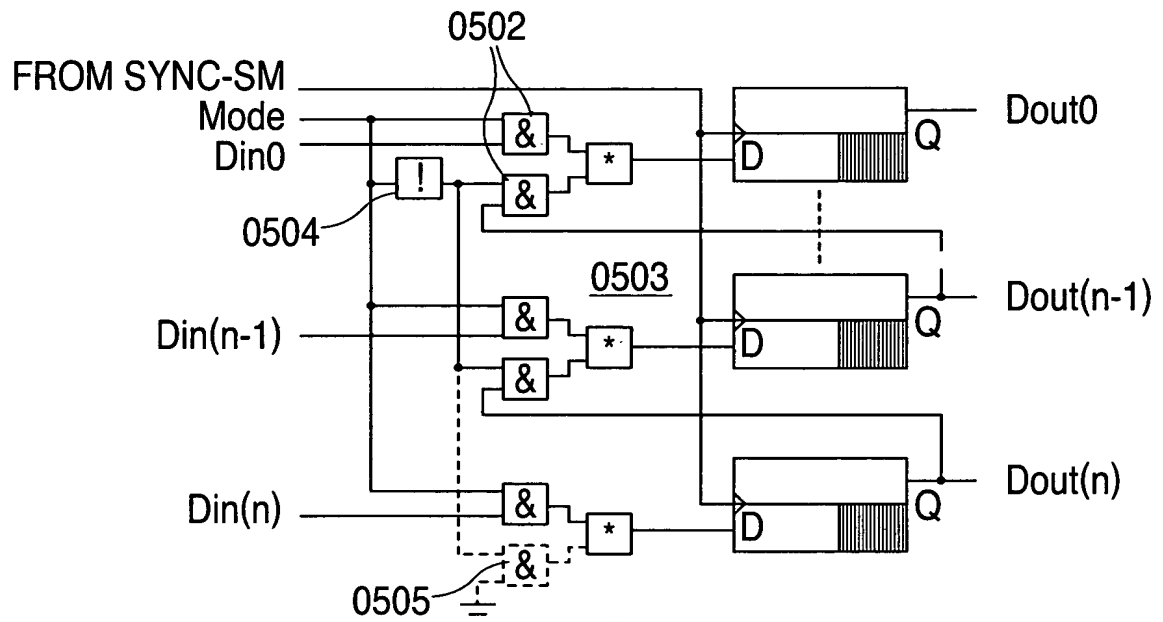


FIG. 5b

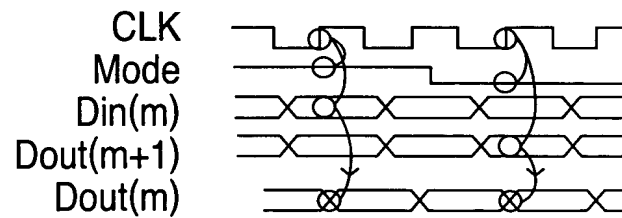


FIG. 5c

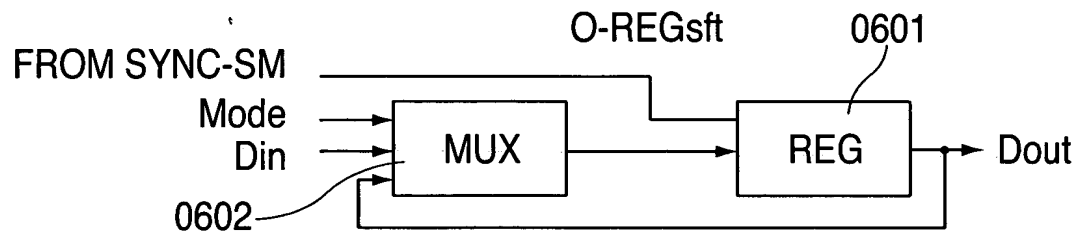


FIG. 6a

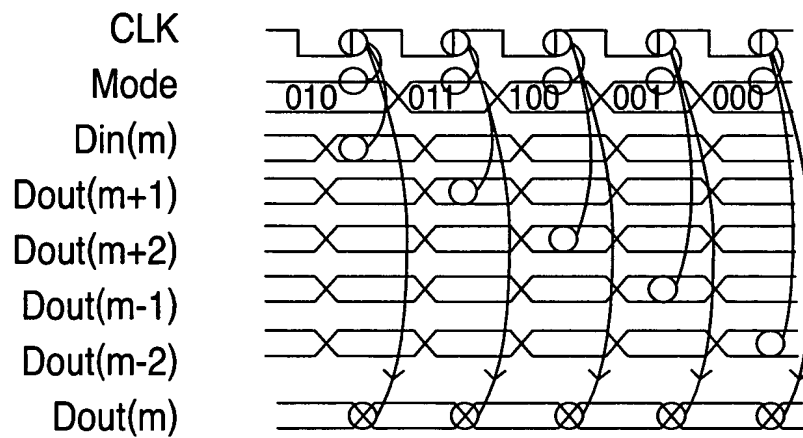


FIG. 6c

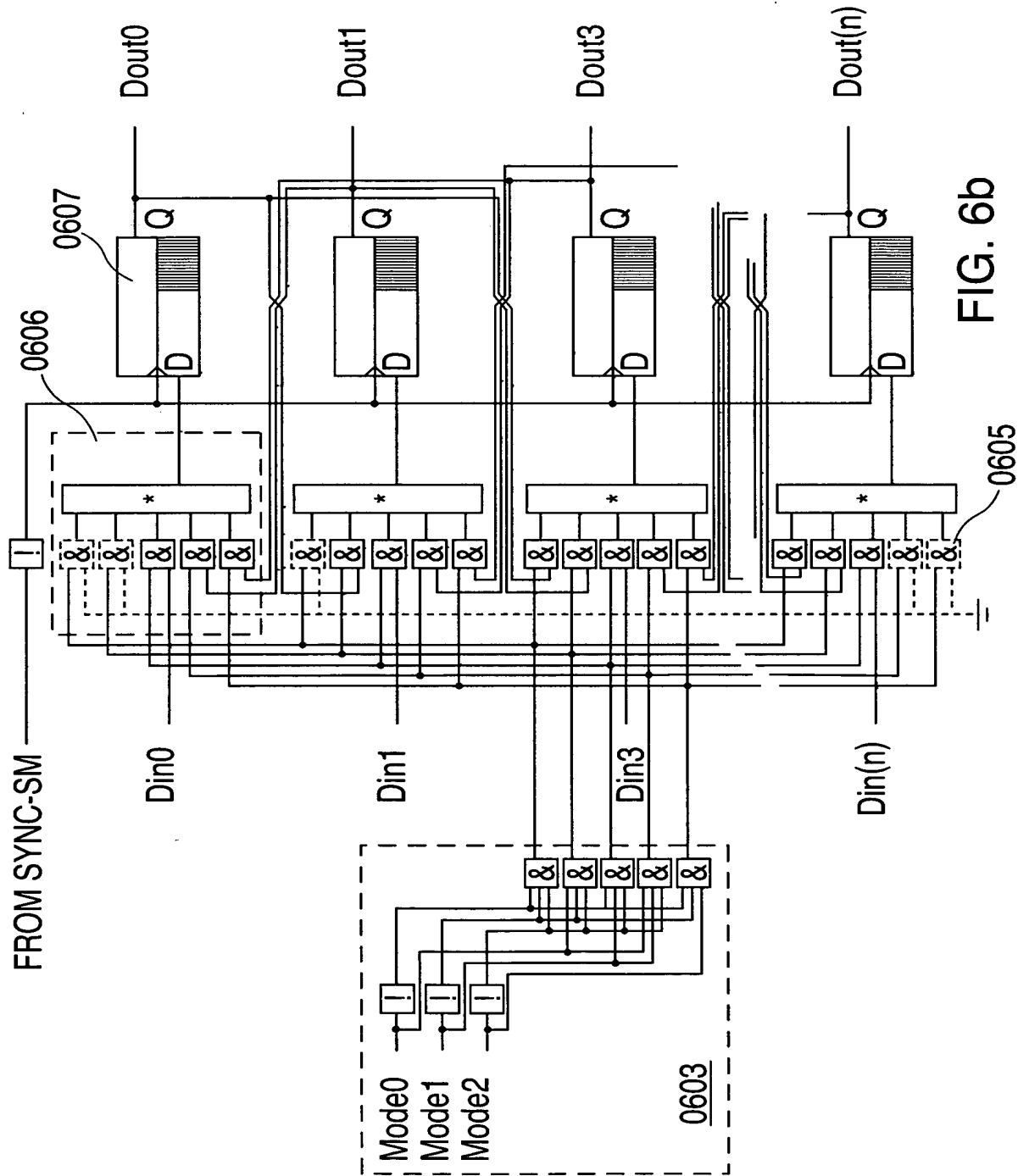


FIG. 6b

8/23

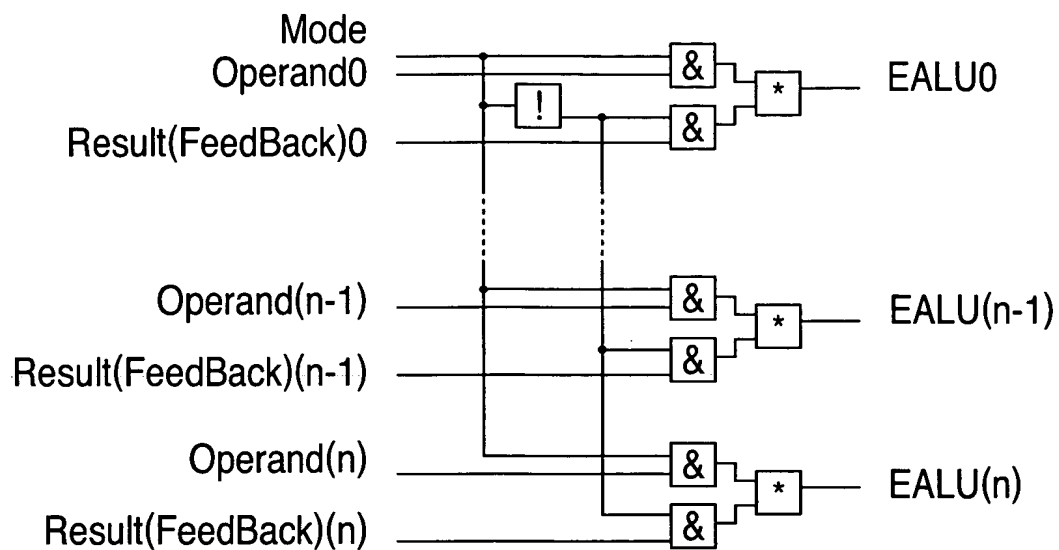


FIG. 7a

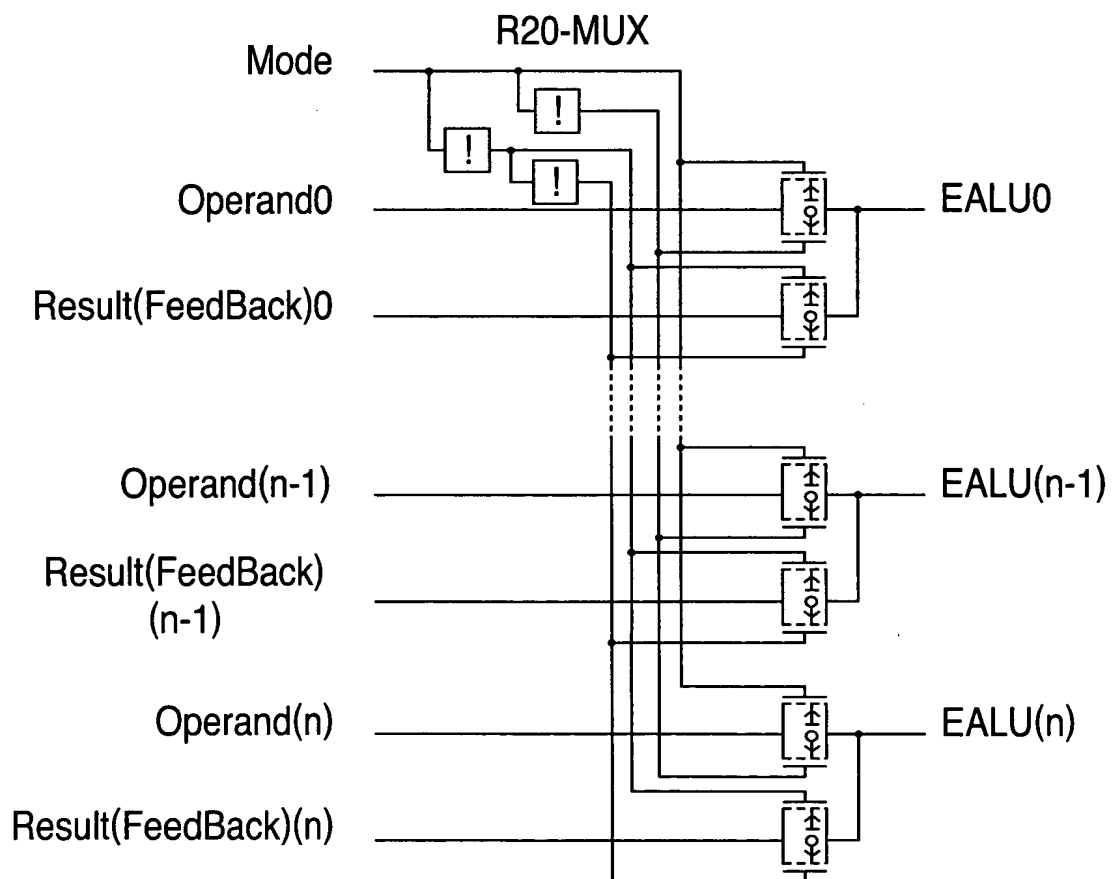


FIG. 7b



# CLOCK SYNCHRONIZATION AND DELAY

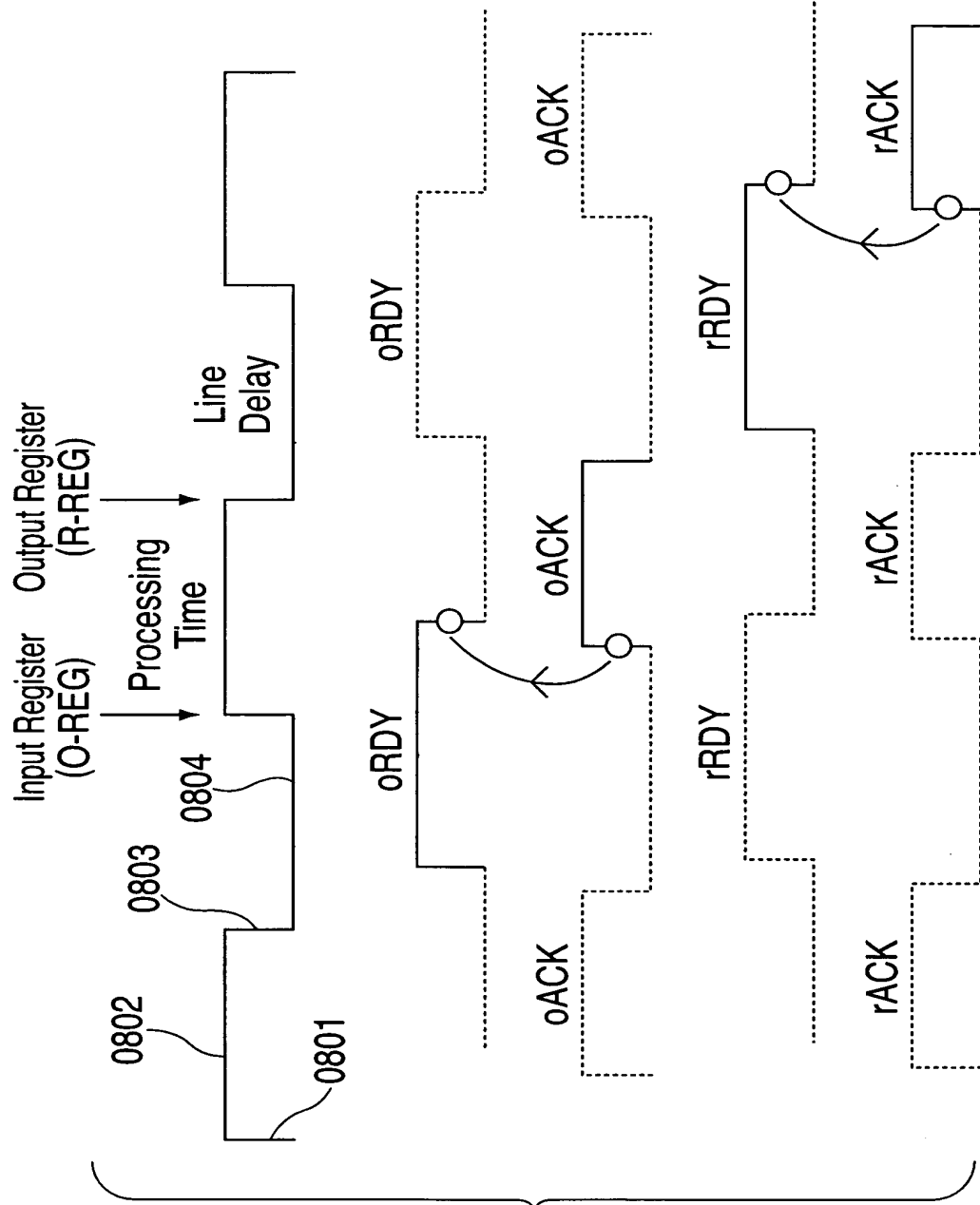


FIG. 8

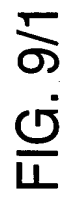


FIG. 9/1

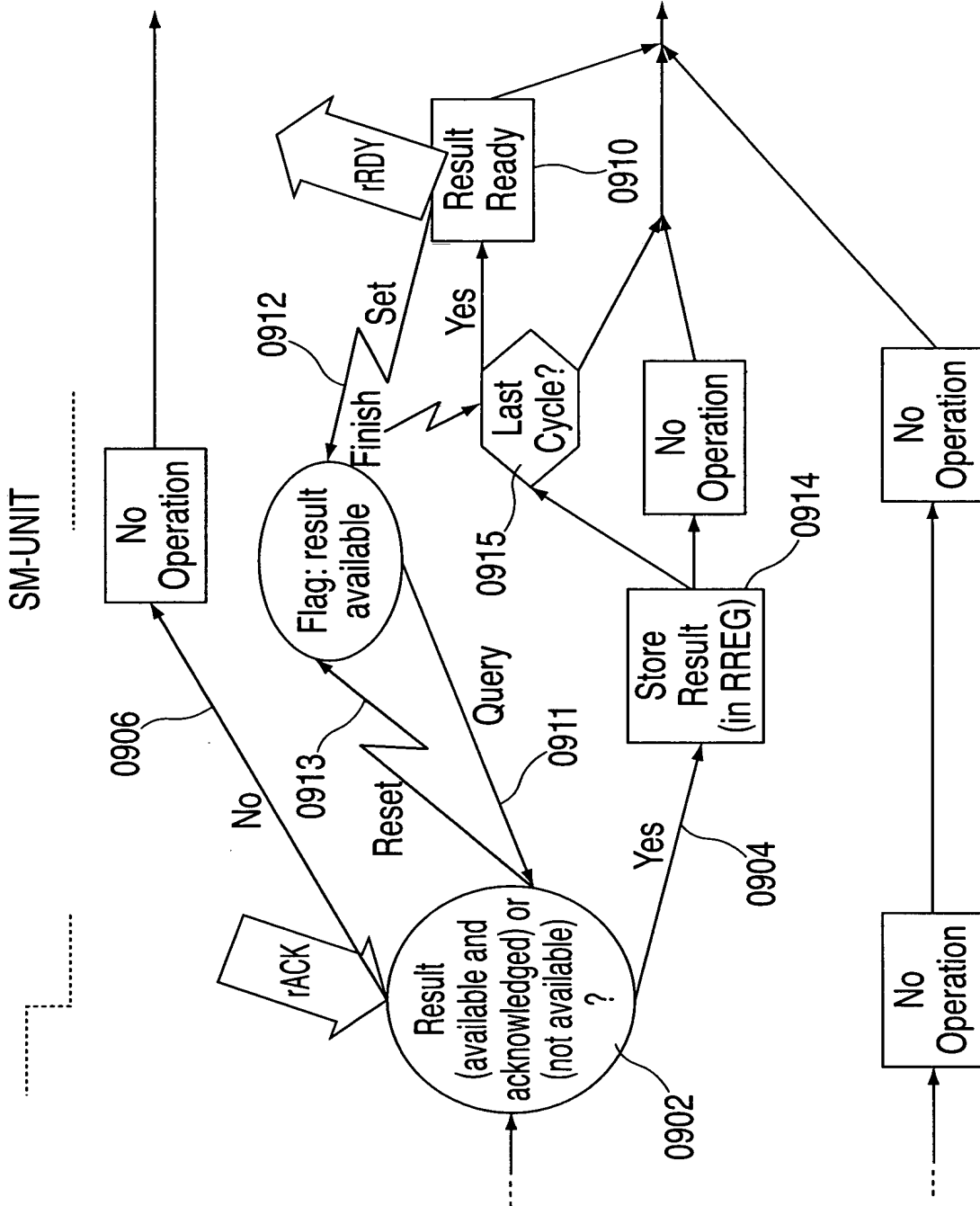


FIG. 9/2

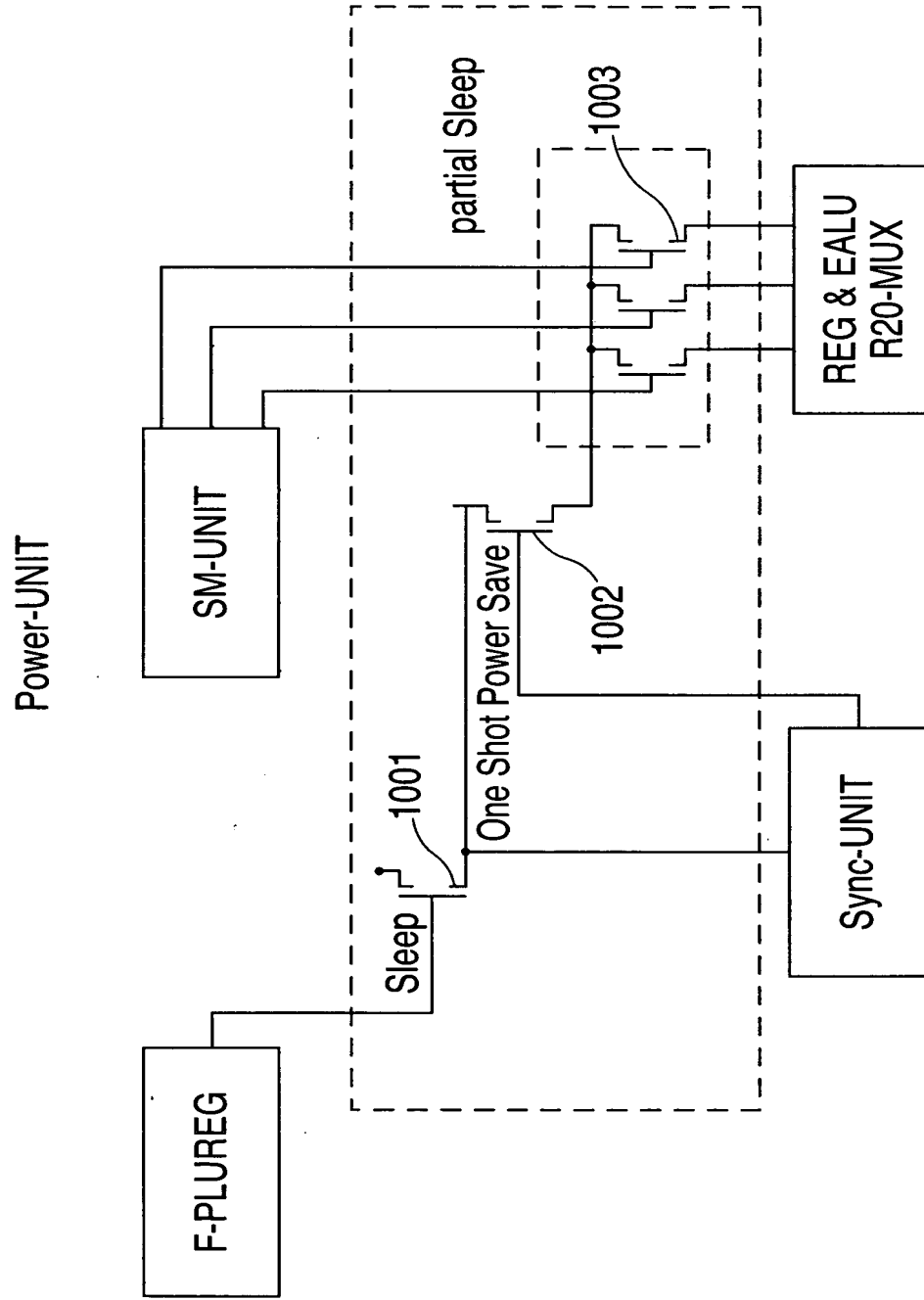


FIG. 10

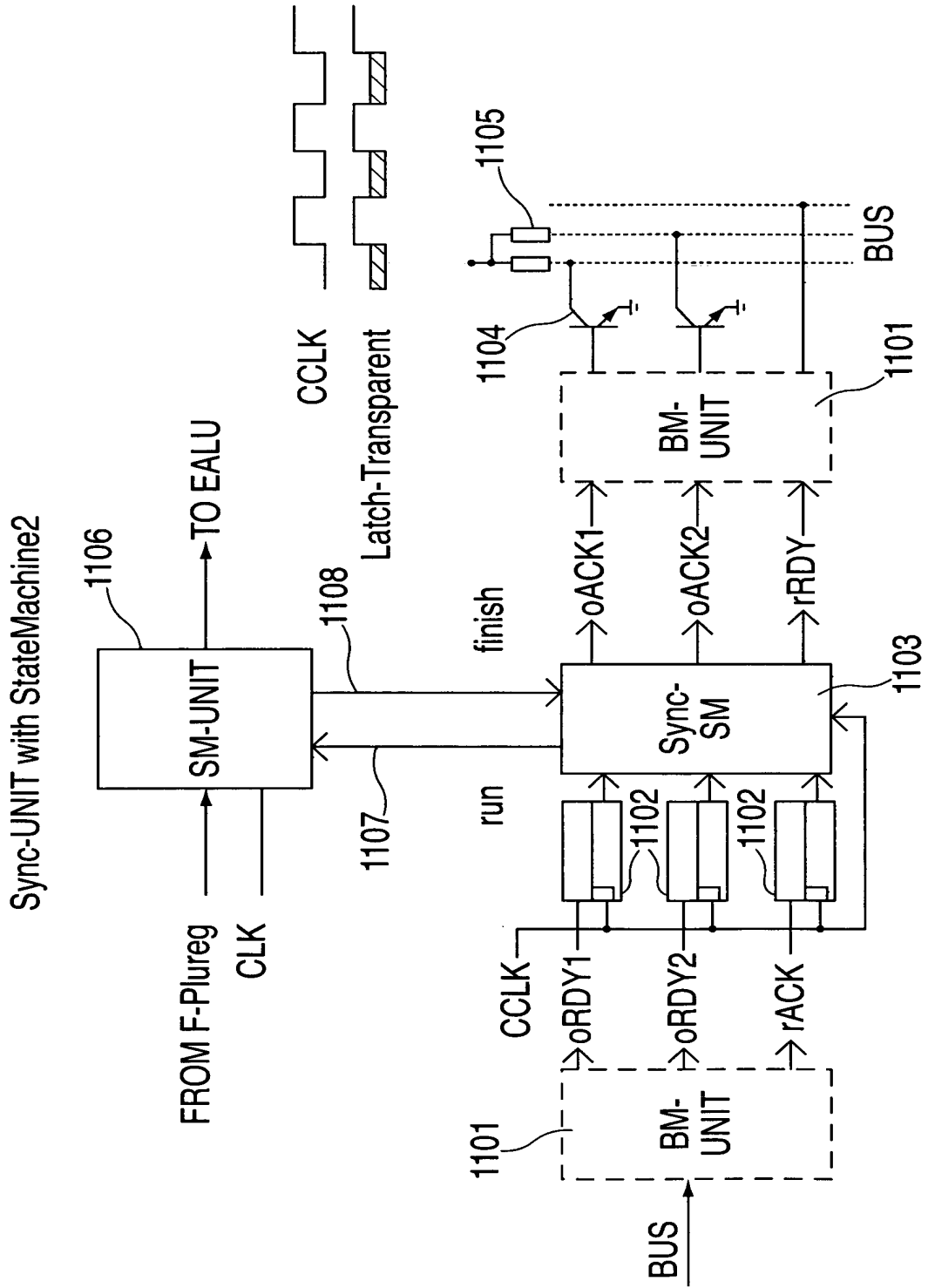


FIG. 11

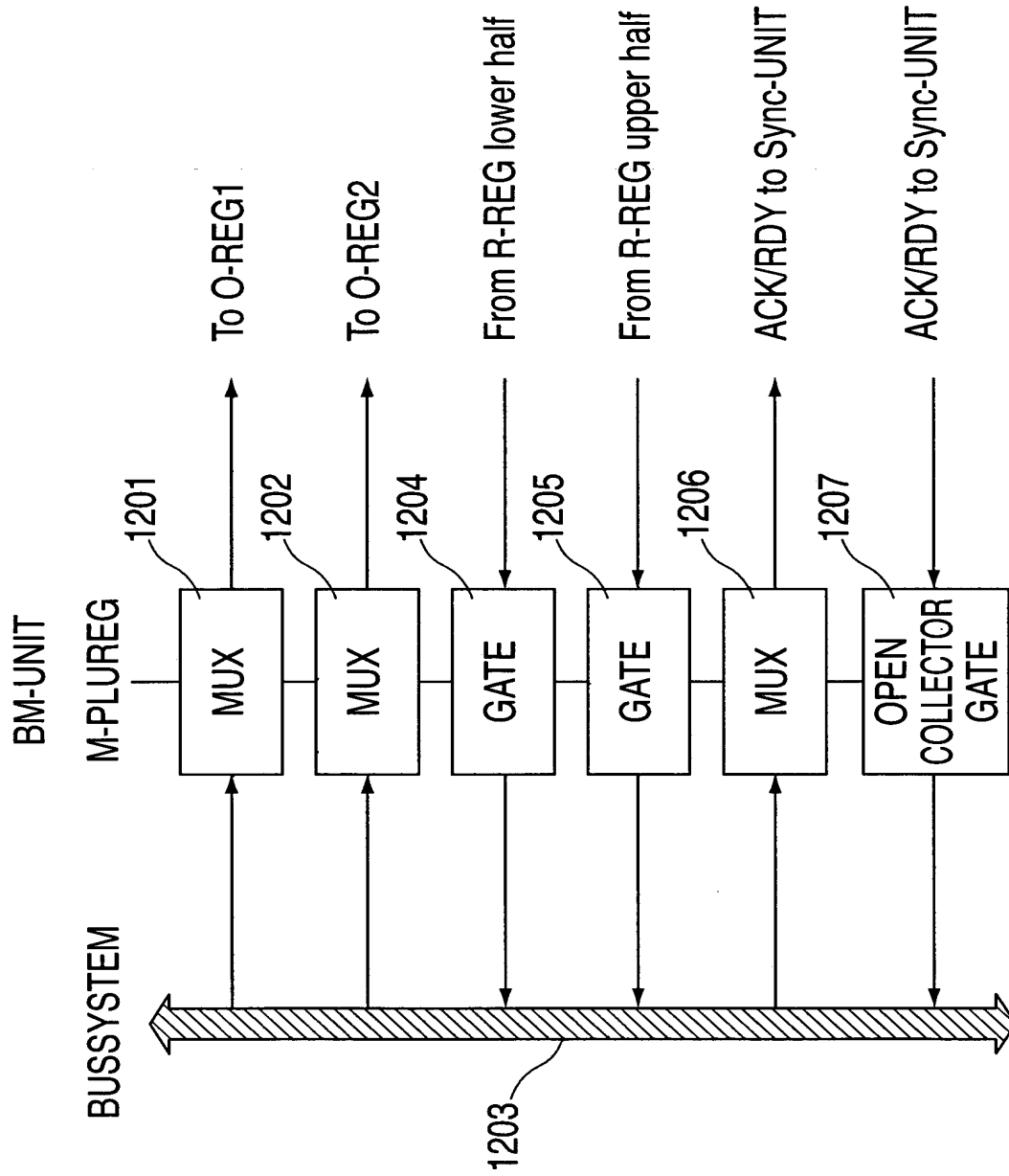
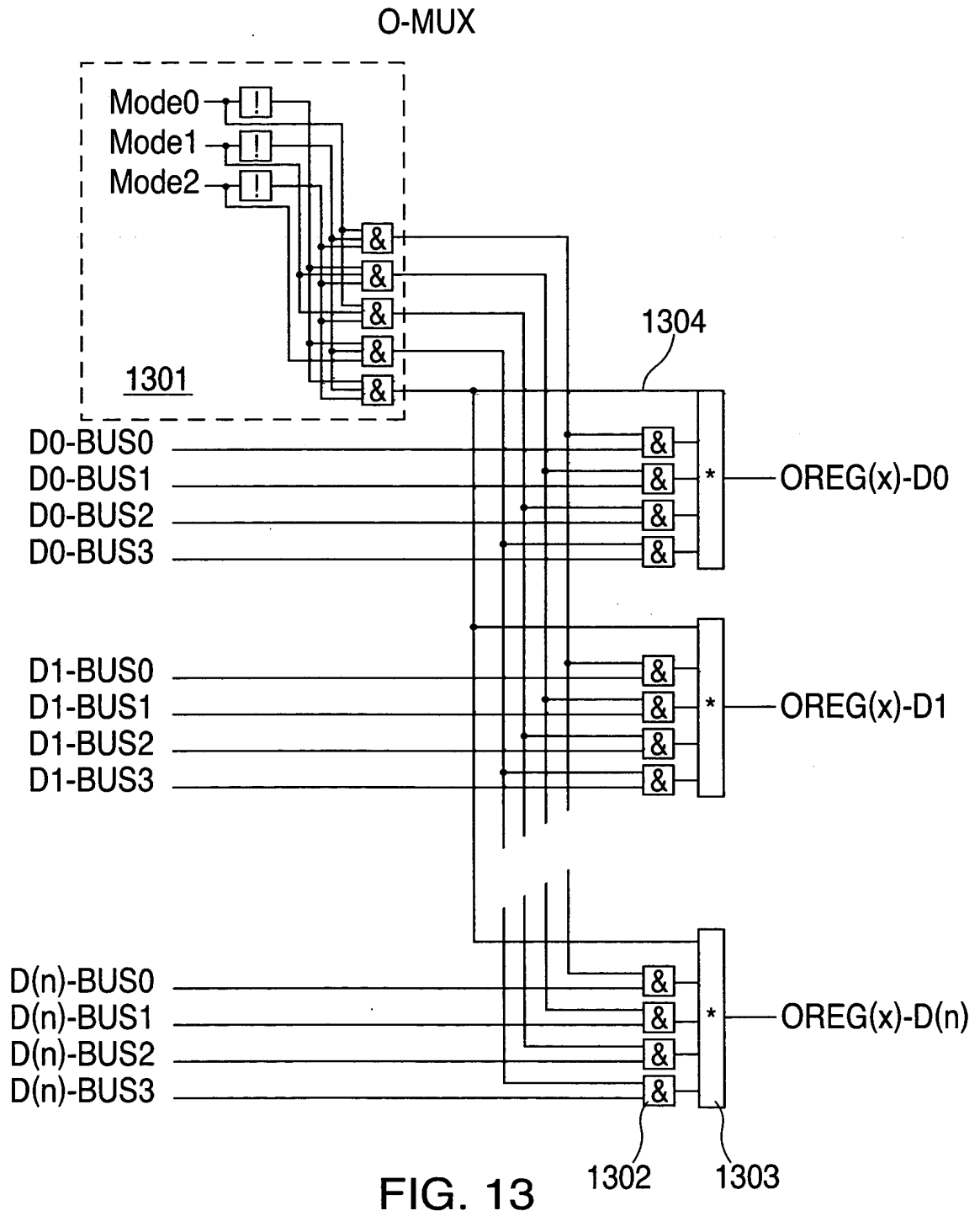


FIG. 12



## R-GATE

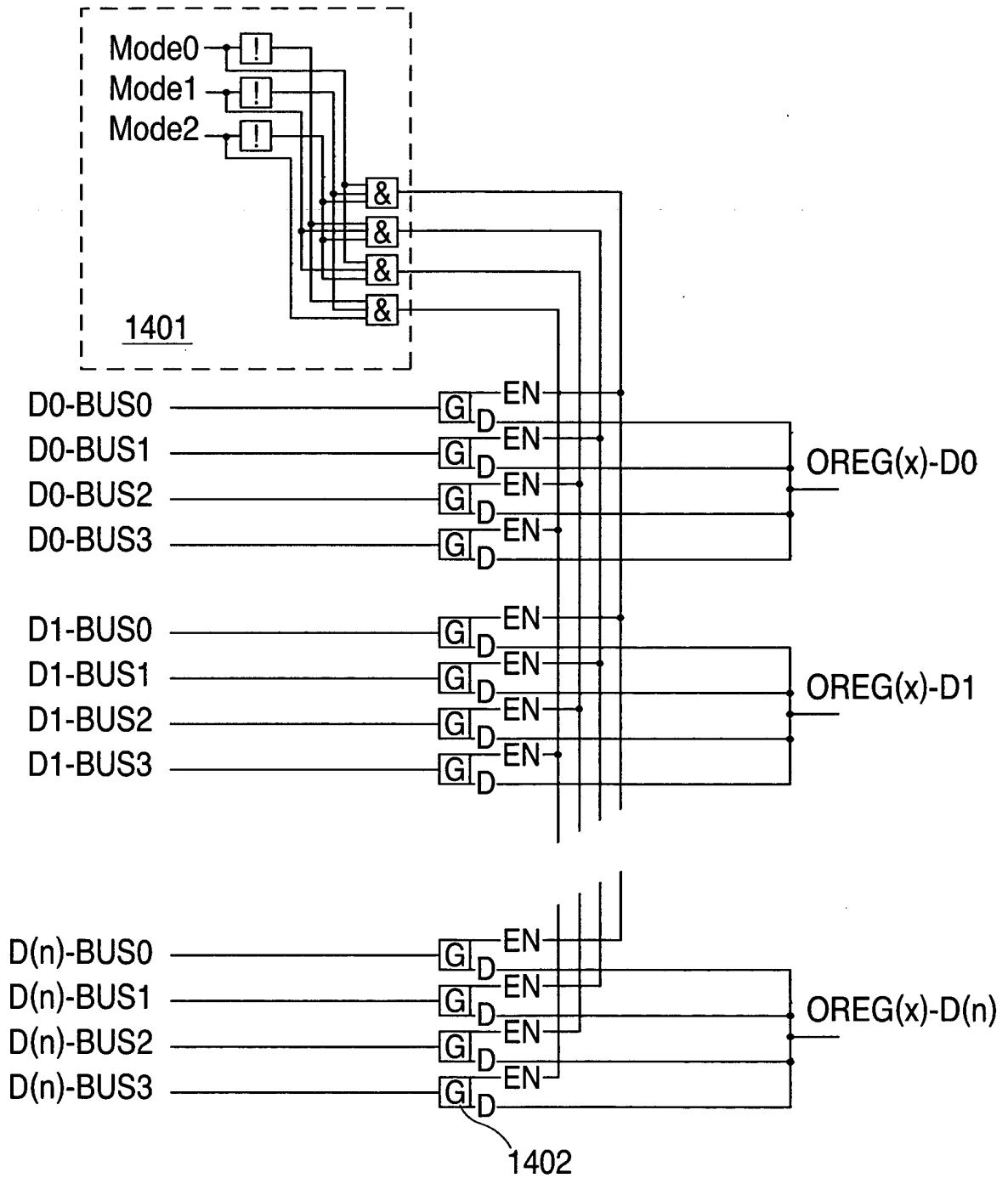
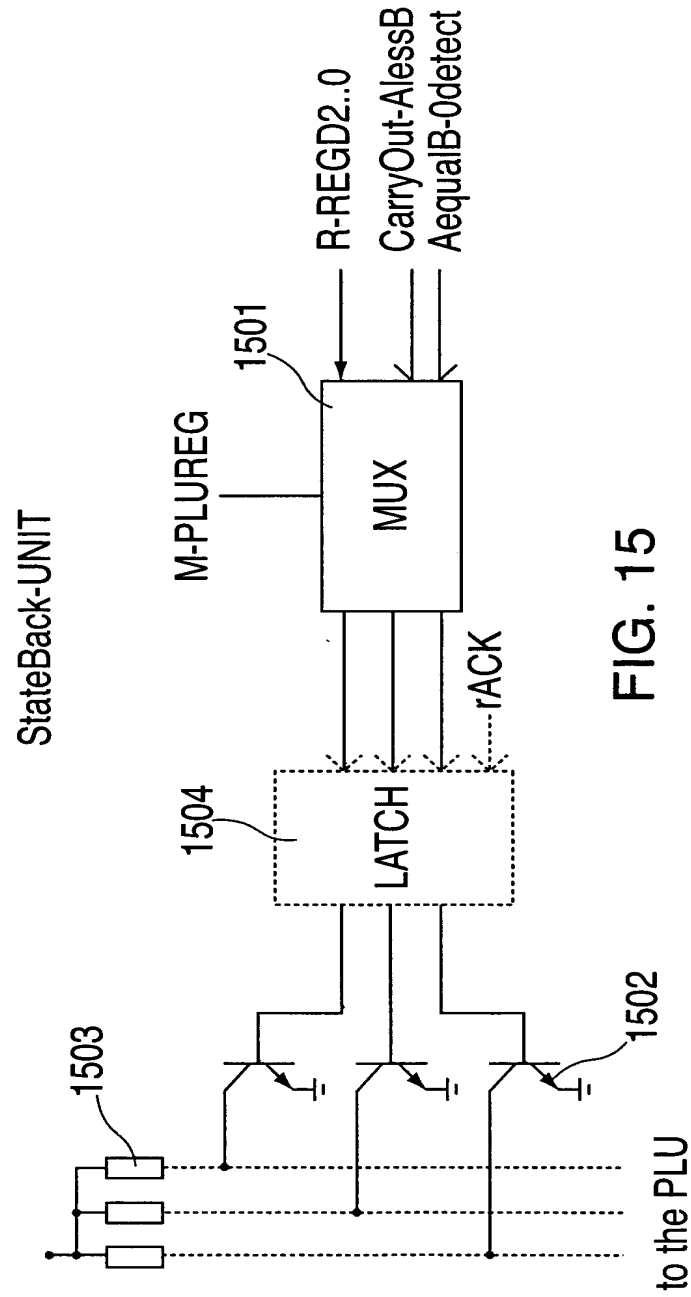


FIG. 14

FIG. 14 is a block diagram of an R-GATE block 1401 and its output drivers 1402.









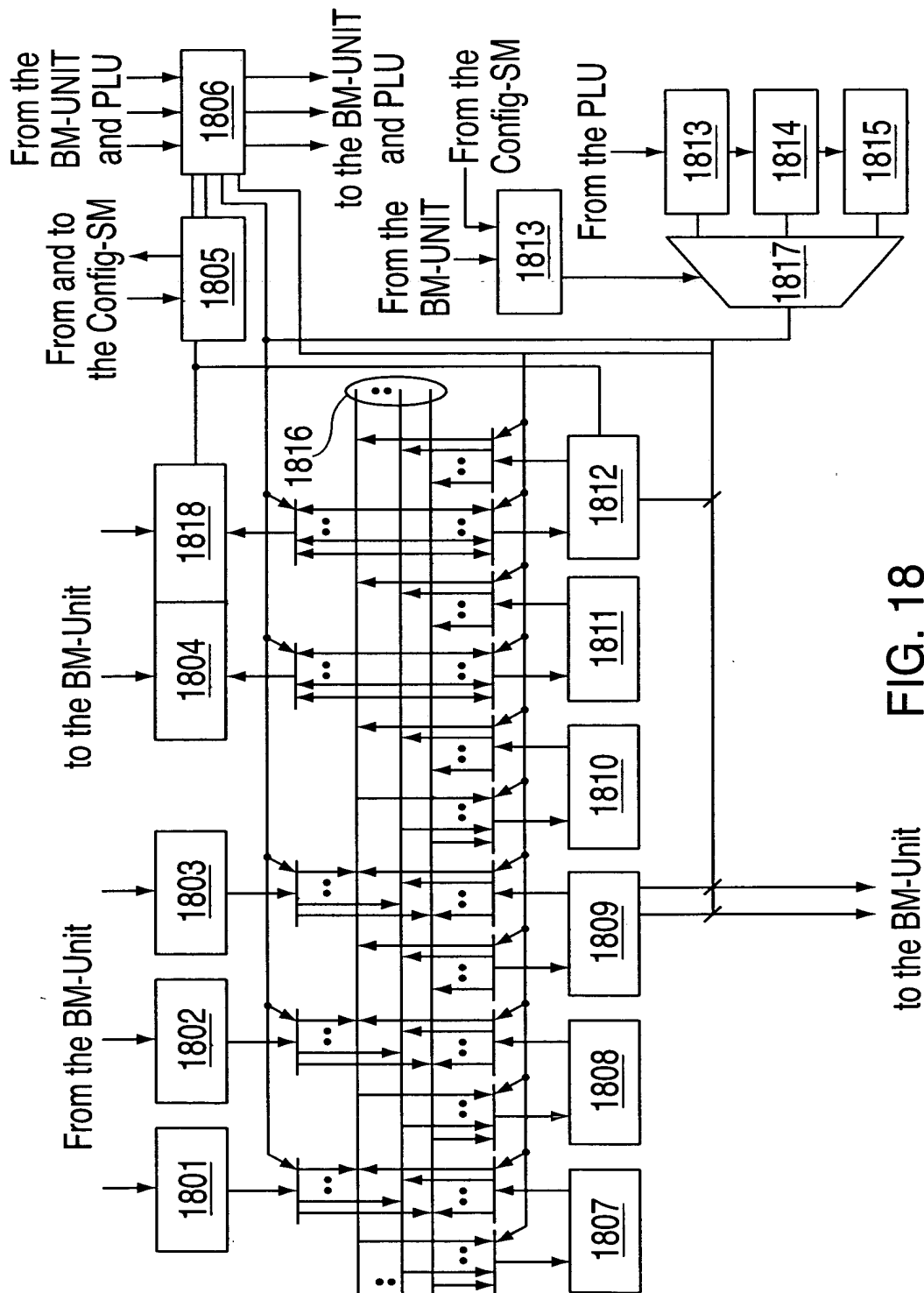


FIG. 18

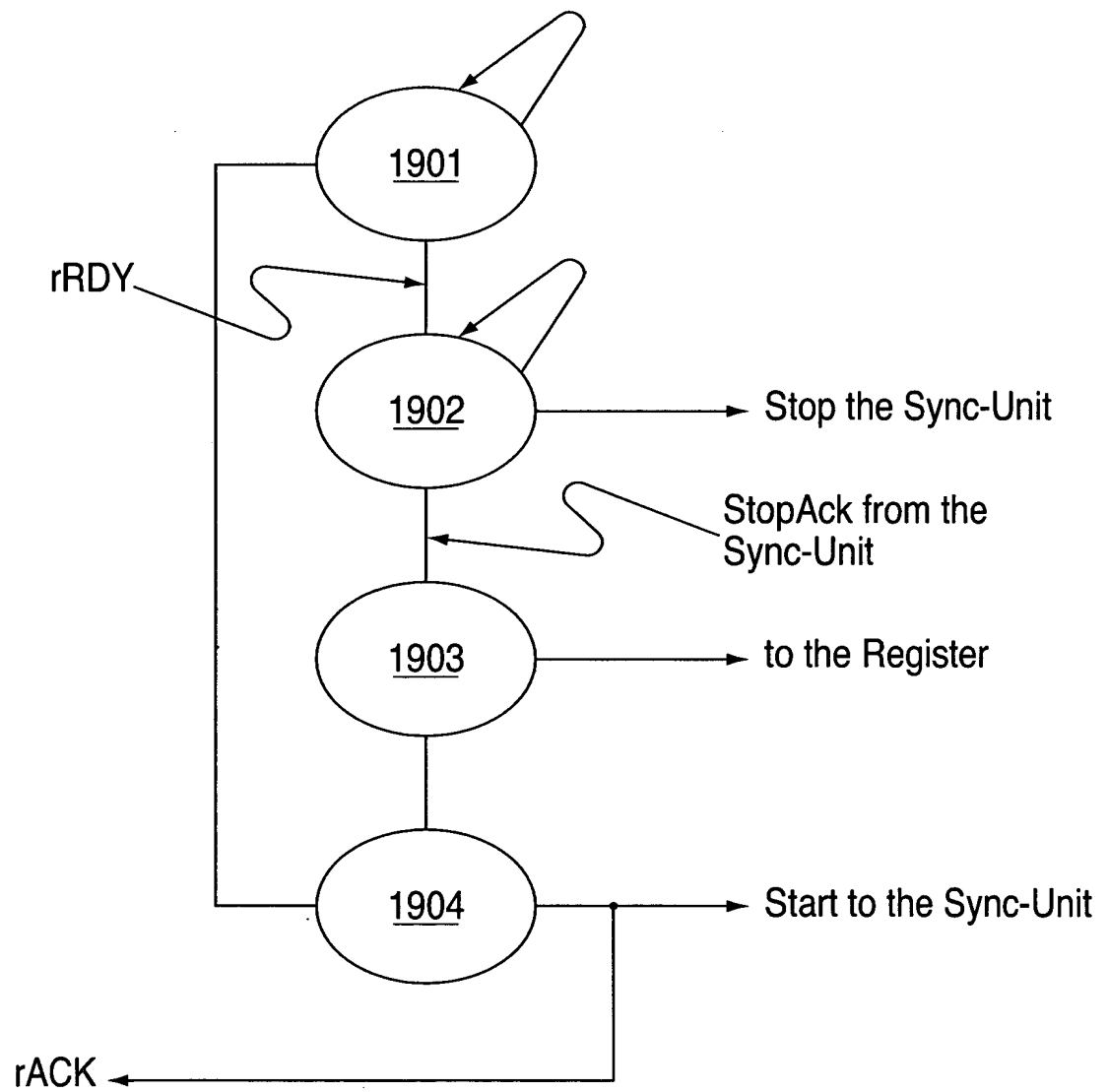


FIG. 19

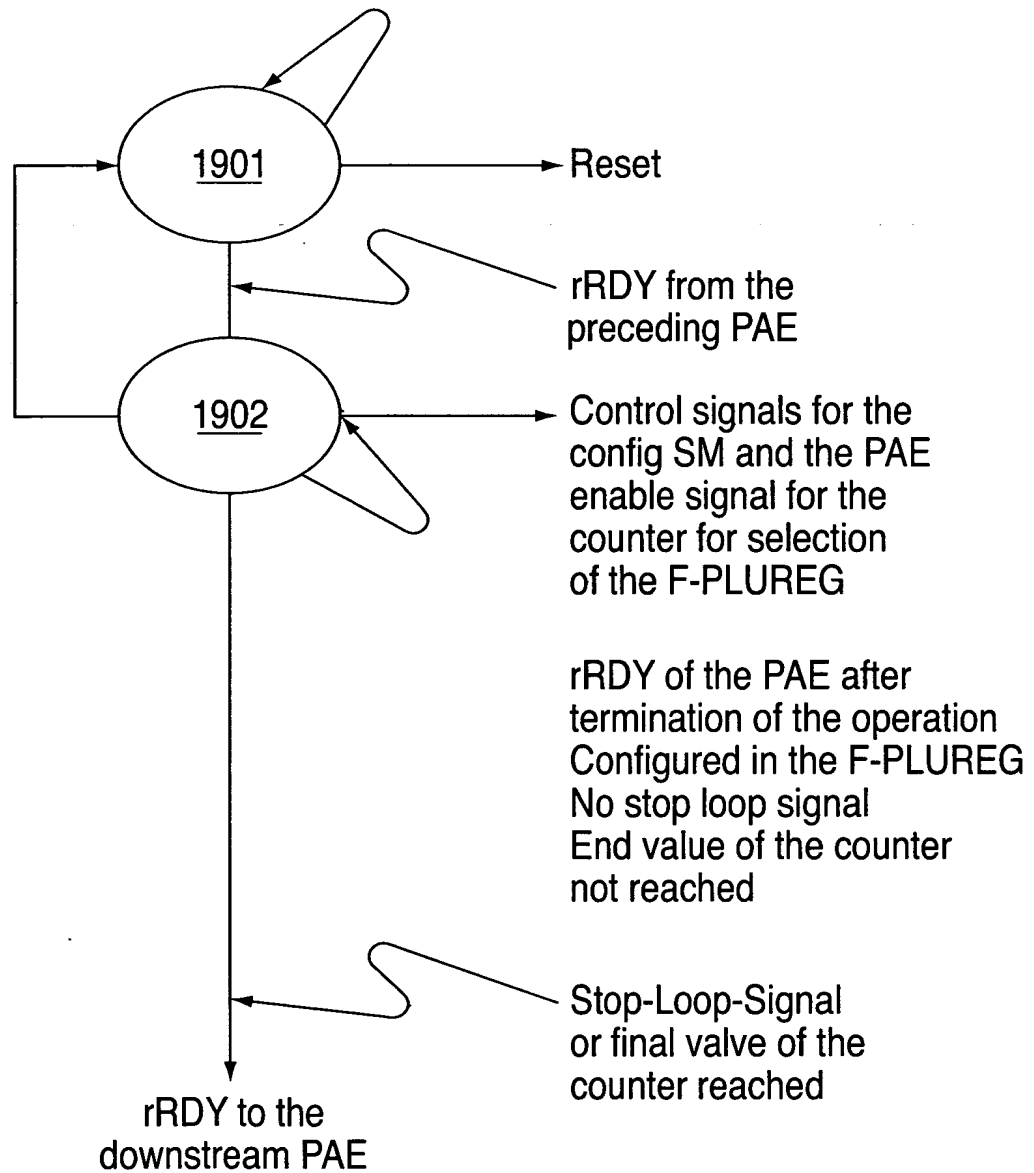


FIG. 20

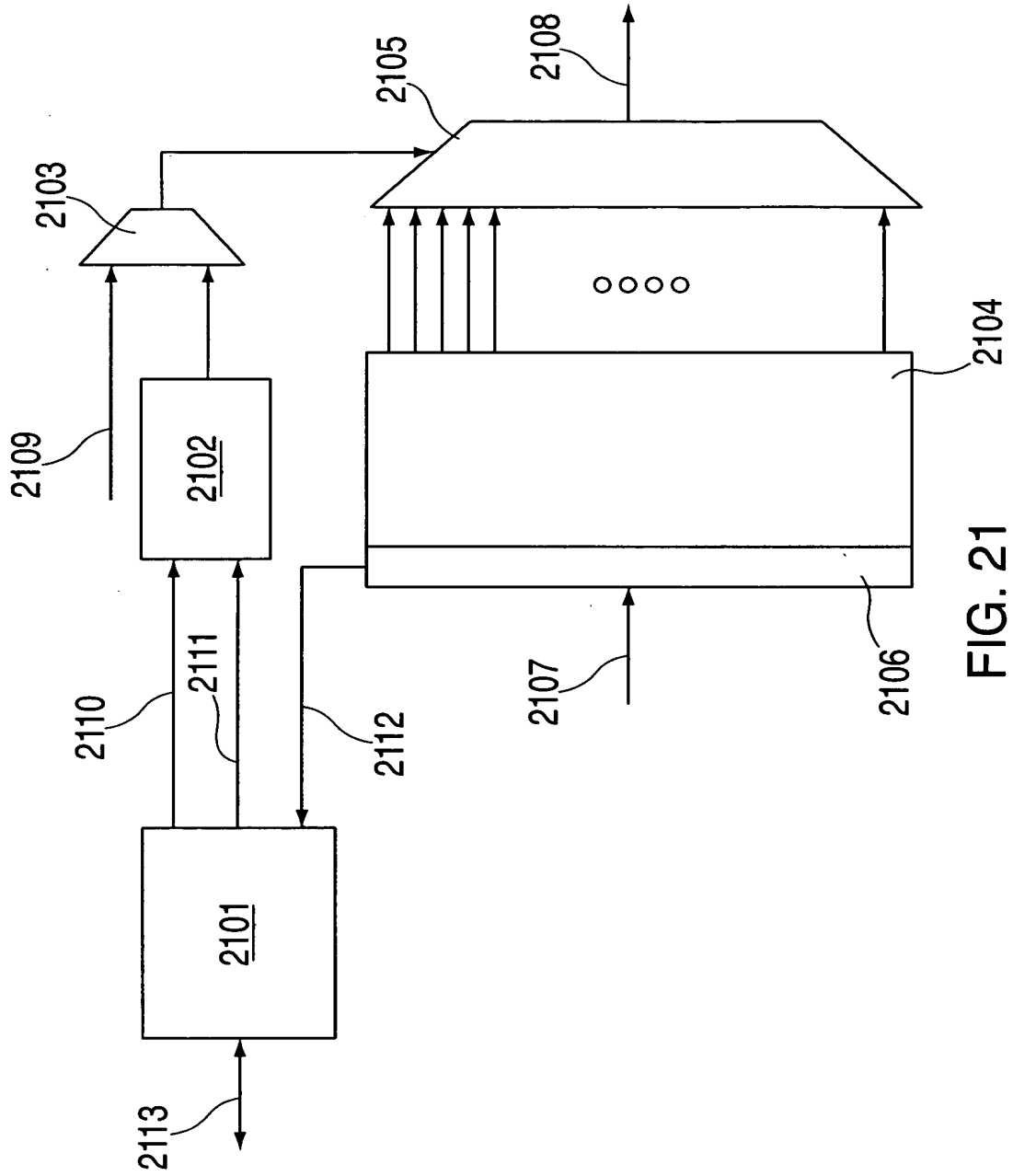


FIG. 21